U.S. Patent Appln. No.: 10/052,779

Amendment dated: June 9, 2003

Reply to Office Action of January 9, 2003

REMARKS

The Office Action dated January 9, 2003 has been carefully reviewed, and these remarks

respond to that Office Action. Applicant respectfully requests reconsideration of the application,

as amended, and allowance of this application.

Applicant acknowledges, with appreciation, the Office's indication that claims 9-11 and

17 in this application contain patentable subject matter.

Upon entry of this Amendment, claims 2, 9-11, 17, 19, 21, and 22 will remain pending in

this application. Claims 1, 3-8, 12-16, 18, and 20 previously were canceled from this application.

Applicant has amended claims 19 and 21 through this Amendment, as described above. No new

matter is included in this Amendment, and no additional claim fees are due as a result of this

Amendment.

Objection to the Drawings

The drawings stand objected to as the Examiner suggests Figure 6 should be modified. In

particular, the Examiner suggests that the drain of transistor 122 of Figure 6 should be shown as

an output rather than ground. Applicant strenuously traverses.

Figure 6 already shows the drain of transistor 122 as an output. Applicant respectfully

draws the attention of the Examiner to the connection between the drain of transistor 122 and the

input of subtractor 114. As to the arrow pointing down from the drain, Applicant respectfully

submits that the arrow is a common identifier for the node leading to a lower voltage. It may be

connected to ground or it may not be connected to ground. If Applicant intended it always be

connected to ground, Applicant would have used the following symbol:

Page 10 of 14

U.S. Patent Appln. No.: 10/052,779 Amendment dated: June 9, 2003

Reply to Office Action of January 9, 2003

\_\_\_\_

Applicant offers to replace the arrow with a dotted line and an arrow if that would clarify

the figure. No meaning different from the current arrow is intended.

Applicant requests the Examiner to withdraw the objection to the drawings.

Rejection Under 35 U.S.C. 112, First Paragraph

Claims 19 and 21 stand rejected under 35 U.S.C. 112, first paragraph. Applicant

traverses.

The Examiner has raised two issues with respect to these claims. First, the Examiner

suggests that at least so sort of input is needed to control the claimed gates. Accordingly,

Applicant has amended each of claims 19 and 21 to recite a voltage applied to a gate.

Second, the Examiner asserts that there are critical elements lacking from the claims.

Applicant respectfully submits that the elements referenced by the Examiner relate to a different

aspect of the present invention. In fact, claims 19 and 21 may or may not be used with the

elements referenced by the Examiner (namely elements 111, 115, 121, and 122). Accordingly, as

other elements may be used, these elements are not critical to the invention as claimed in claims

19 and 21. Accordingly, the specific elements as listed by the Examiner are not specifically

listed as they are not critical to the invention as claimed.

Rejection Under 35 U.S.C. 112, Second Paragraph

Claims 19 and 21 stand rejected under 35 U.S.C. 112, second paragraph. Applicant

traverses.

Page 11 of 14

U.S. Patent Appln. No.: 10/052,779

Amendment dated: June 9, 2003

Reply to Office Action of January 9, 2003

The Examiner argues that there are no connections between the "subtractors to the gate

and drain of the 'first transistor'." Applicant respectfully notes that there is no connection

between the subtractors and the gate and drain of the first transistor. Rather, as recited in claim

19, for example:

more than one subtracter, each subtracter coupled to the

gate of a corresponding compensation PMOS transistor..."

Accordingly, the subtractor is connected to the gate of the PMOS transistor, not to the

first transistor. Applicant further notes that the claims specify how the first PMOS transistor is

connected to each compensation PMOS transistor.

As to the rejection of "drain-source voltage" and "gate-source voltage," Applicant has

amended the claims to recite a voltage applied to the gate, thereby rendering clear these

recitations.

Applicant respectfully submits that the claims are clear as drafted. Applicant requests that

the rejection of these claims be withdrawn.

Rejection Over Guliani

Claims 2 and 22 stand rejected under 35 U.S.C. 102(b) over Guliani. Applicant traverses.

The Examiner alleges that "Guliani discloses ... a circuit comprising ... 'at least one

compensation PMOS transistor' ... connected and operating similarly as recited by Applicant."

This statement is incorrect.

The Examiner has attempted to find three transistors (here, transistors 42, 32 or 44, and

16) and argues that, because the three transistors exist, they must function the same as claimed.

Page 12 of 14

U.S. Patent Appln. No.: 10/052,779 Amendment dated: June 9, 2003

Reply to Office Action of January 9, 2003

However, claim 2 recites, inter alia:

" a compensation circuit coupled to the drain of the first

MOS transistor and the drain of the second MOS transistor, the

compensation circuit configured to decrease the mirror current

against an increase of absolute value of a drain voltage of the

second MOS transistor such that the mirror current and a current

flowing into the first MOS transistor are the same."

There is nothing in Guliani that discloses the compensation that functions as recited.

Rather, Guliani discloses that the circuit of Figure 2 is to maintain the operating voltage V1 at a

desired value despite fluctuations in supply voltage:

"W-channel device 16 is coupled to the current mirror section 30

for maintaining the operation point of the circuit 20 in accordance

with the diagram in FIG. 3." See column 5, lines 36-38.

There is nothing in Guliani that discloses decreasing the mirror current of the current

mirror while there is an increase in the absolute value of a drain voltage of the second MOS

transistor. On the contrary, Guliani attempts to keep the voltage constant despite any fluctuations

in the current through the current mirror. See specifically, Figure 3 where the system maintains a

relatively constant voltage despite an increasing current.

The system recited in claim 2 handles the current and voltage differently:

"decrease the mirror current against an increase of absolute value

of a drain voltage of the second MOS transistor"

Claim 22 is similar.

U.S. Patent Appln. No.: 10/052,779 Amendment dated: June 9, 2003

Reply to Office Action of January 9, 2003

Guliani fails to disclose the functions as claimed in claims 2 and 22. Accordingly, claims 2 and 22 are allowable over Guliani.

If any additional fees are due along with this paper, the Commissioner is authorized to debit our Deposit Account No. 19-0733 to cover any necessary fees. Also, if an extension of time is needed that is not accounted for in this Amendment or any accompanying papers filed with it, the necessary extension is requested. Please charge the extension fee to Deposit Account No. 19-0733.

All rejections having been addressed, Applicant respectfully submits that this application is in condition for immediate allowance and respectfully solicits prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

By:

Registration No. 38,800

1001 G Street, N.W.

Washington, D.C. 20001-4597

Tel: Fax: (202) 824-3000 (202) 824-3001

Dated: June 9, 2003